IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Jerrell Hein et al.		
Title:	CALIBRATON OF OSCILLATOR DEVICES		
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APPEAL BRIEF (37 C.F.R. § 41.37)

This brief is in furtherance of the Notice of Appeal, filed on January 19, 2006. A Two Month Extension of Time is being submitted herewith to extend the time for filing this Appeal Brief to May 19, 2005. The fee required under 37 C.F.R. § 41.20(b)(2) is being submitted herewith.

REAL PARTY IN INTEREST

The real party in interest in this appeal is Silicon Laboratories Inc, the assignee of record.

RELATED APPEALS AND INTERFERENCES

There are no known prior and pending appeals, interferences or judicial proceedings which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-7 and 10-48 are pending and stand rejected. Rejected claims 1-7 and 10-48 are the subject of this appeal.

STATUS OF AMENDMENTS

An amendment to claim 10 was filed subsequent to the final rejection to correct an antecedent basis problem. The Advisory action does not indicate that the amendment was entered for the purposes of appeal (or that the amendment was not entered) but Applicants presume that was an oversight by the Examiner, and given its nature, that the amendment will be entered for purposes of appeal.

SUMMARY OF CLAIMED SUBJECT MATTER

A concise explanation of the subject matter defined in each of the independent claims involved in the appeal is set forth below. Each independent means plus function claim is identified below and the structure, material, or acts described in the specification as corresponding to each claimed function is set forth below.

The independent claims are directed to calibration of oscillator devices. Calibration according to an embodiment of the invention is described in paragraphs 1045-1051. An overview of an embodiment of the calibration operation is as follows. Referring to Figs. 3 and 4, in an embodiment, the control circuit 30 receives a command indicating that a calibration clock is to be supplied over the serial port (input/output terminal 27, P1, or P2). Subsequently, the calibration clock is supplied as an input frequency reference for the calibration PLL. The calibration PLL is a control loop formed by phase detector and loop filter 51, digitally controlled oscillator (DCO) 39 and the feedback path through divider 37 and multiplexer 47. In response to the write command, the control state machine selects the A input for multiplexer 47 (from the digital phase detector and loop filter 51), to form the phase-locked loop with DCO 39. The received calibration clock is supplied via node 53 to the divider circuit 35. The digital phase detector 51 detects the phase/frequency difference between the calibration clock and the output (f_{OSC}) of the DCO 39 and provides a correction signal 58 to summer 49 through multiplexer 47 to adjust the control signal M supplied to the DCO 39 on node 50 to reflect that difference.

The calibration clock is applied for sufficient amount of time to allow the PLL to settle and establish the correction factors needed to lock the DCO 39 output clock (f_{OSC}) to a multiple of the low frequency input calibration clock. The DCO may lock to an integer or fractional

multiple (e.g., a ratio or integers) of the calibration clock according to the dividers utilized. Note that because of the divider 37 in the feedback path of the PLL, the calibration clock can be a low frequency signal even for those devices with high speed output clocks. As described in paragraph 1049 once the PLL is locked and settled, the internal state of the device is stored, thereby calibrating the device to the input calibration clock. The value stored may be the value M supplied to the DCO or a correction factor supplied on node 58. The value(s) are stored in a non-volatile memory 60.

Claim 42 is in means plus function format. The claim recites a terminal for receiving a signal. Fig. 4 and paragraph 1048 describe terminals 27, P1, and P2 receiving a calibration clock. The claim further recites a resonating device supplying a reference signal having a fixed frequency. Figs. 3 and 4 show, e.g., crystal oscillator or SAW 11. The claim further recites a controllable oscillator coupled to receive the reference signal and generate a clock signal. Fig. 8 shows DCO 39 receiving an input 800 from the crystal or SAW 11. That is also shown in Fig. 4.

The claim also recites means for calibrating the apparatus utilizing a calibration clock supplied on the terminal by internally generating, in a phase-locked loop, one or more control values for the controllable oscillator to cause the oscillator to output a signal corresponding to the calibration clock; and a non-volatile storage storing one or more values corresponding to the one or more control values. The structure, material, or acts corresponding to the claimed function is described in Figs. 3, 4, 7, and 8 and in paragraphs 1045-1051. With reference to Fig. 4 and paragraph 1048, a calibration clock is received at P1 or P2. In response to a command, the control state machine selects the A input for multiplexer 47 (from the digital phase detector and loop filter 51), to form the phase-locked loop with DCO 39. The DCO corresponds to the claimed controllable oscillator. The calibration clock (CALCK) is supplied via node 53 to the divider circuit 35. The digital phase detector and loop filter 51 detects the phase/frequency difference between the calibration clock and the output of the DCO 39 (f_{OSC}) and provides a correction signal 58 to summer 49 through multiplexer 47 to adjust the control signal M supplied to the DCO 39 to reflect that difference. The calibration clock is applied for sufficient amount of time to allow the PLL to settle and establish the correction factors needed to lock the DCO 39 output clock to an integer multiple of the low frequency input calibration clock. The calibration

may be performed at multiple temperatures. In that way one or more control values are generated to cause the controllable oscillator to output a signal corresponding to the calibration clock, thereby calibrating the apparatus. As described in paragraph 1049 once the PLL is locked and settled the internal state of the device is stored. The value stored may be the value M supplied to the DCO or a correction factor supplied on node 58. The value(s) are stored in a non-volatile memory 60. Finally, the claim recites a non-volatile storage storing one or more values corresponding to the one or more control values.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Ground I: The rejection of claims 1, 2, 6, 7, 10, 16, 17, 19, 21, 22, 26-28, and 42 under 35 U.S.C. § 102(b) as being anticipated by Walker et al. (U.S. Patent No. 5,579,348) (hereinafter Walker).

Ground II: The rejection of claims 3-5, 20, and 44-47 under 35 U.S.C. § 103(a) as being unpatentable over Walker et al. in view of Sutardja (U.S. Pub. 2004/0071029).

Ground III: The rejection of claims 11-15, 18, 20, 23-25, 29-41, 43 and 48 under 35 U.S.C. § 103(a) as being unpatentable over Walker et al. in view of Torode (U.S. Patent No. 5,451,912).

ARGUMENT

Ground I: The rejection of claims 1, 2, 6, 7, 10, 16, 17, 19, 21, 22, 26-28, and 42 under 35 U.S.C. § 102(b) as being anticipated by Walker.

Claims 1, 2, 6, 7, 10, 16, 17, 19, 21, 22, 26-28, and 42

Independent claims 1, 21, 26, and 42 all recite a non-volatile memory or storing into a non-volatile memory. With regard to claim 1, the final Office action states that "[i]t is inherent that the memory 62 [of Walker] is nonvolatile because of is functionality of data usage and handling." Applicants respectfully disagree that the memory 62 in Walker is inherently non-volatile. Under 35 U.S.C. § 102(b), each element of a claim must be found in the single prior art reference, either expressly or inherently. See Minnesota Min. & Mfg. Co. v. Johnson & Johnson

Orthopaedics, Inc., 976 F.2d 1559, 1565, 24 USPQ2d 1321, 1326 (Fed. Cir. 1992). A reference teaches an element inherently if the "prior art necessarily functions in accordance with, or includes, the claimed limitations." See MEHL/Biophile Int'l Corp. v. Milgraum, 192 F.3d 1362, 1364, 52 USPQ2d 1303, 1305 (Fed. Cir. 1999). If the reference fails to teach even one limitation of a claim, then the claim is not anticipated. See Kloster Speedsteel AB v. Crucible Inc., 848 F.2d 1560, 7 USPQ2d 1507 (Fed. Cir. 1986).

While a teaching may be express or inherent, as described above, inherency is a stringent standard.

> To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Continental Can Co. v. Monsanto Co., 948 F.2d 1264, 1268, 20 USPQ2D 1746, 1749 (Fed. Cir. 1991). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." Id. at 1269, 20 USPQ2D at 1749 (quoting In re Oelrich, 666 F.2d 578, 581, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981).

See In re Robertson, 169 F.3d 743, 745; 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). Appellants respectfully disagree that the memory in Walker inherently non-volatile. There is nothing in Walker that requires or even suggests that the memory 62 is non-volatile. There is no teaching that the memory should be maintained while the device is off. There is no reason that the memory 62 in Walker has to maintain its contents while the other components of the clock recovery circuit shown in Figs. 1-3 are powered off. Walker teaches

> a method and apparatus for improving the apparent accuracy of a relatively inaccurate data receiver master clock in order to reduce the acquisition time of a desired information signal. The receiver master clock is first calibrated using an accurate timing relationship inherent in a received signal. The detected timing relationship is more accurate than the accuracy of the master clock itself. After calibration, a timing component of the desired information signal is acquired and used to run the master clock in a conventional

Col. 6, lines 24-36. Walker teaches that an initial value is determined for memory 62. There is nothing in reducing the acquisition time of a desired information signal using a received signal that necessarily requires a nonvolatile memory. If a non-volatile memory were required or

preferred in Walker, the patent would presumably identify that characteristic of the memory. There is simply no teaching in Walker (or need in Walker) for the memory 62 to be nonvolatile. Since that is the case, it is clear that the memory 62 of Walker is not inherently non-volatile. Accordingly, Applicants respectfully request that the rejection of claims 1, 21, 26, and 42, and all claims dependent thereon, as anticipated by Walker, be reversed.

Claim 10

Claim 10 (amended to provide for correct antecedent basis to claim 1) recites *supplying a fixed frequency reference from a fixed frequency reference source.* The Office action states that Walker teaches in column 3, lines 60-63, a fixed frequency reference source to synthesize the output clock. Applicants respectfully disagree. Walker teaches at col. 3, lines 60-67 that a transmitted reference signal such as a horizontal sync or color burst pulse inherent in a broadcast television signal can be used for controlling the master clock to operate with an improved range of accuracy. Applicants respectfully submit that a broadcast television signal is not a fixed frequency reference source and therefore Walker does not teach *supplying a fixed frequency reference from a fixed frequency reference source.* Accordingly, Applicants respectfully request that the rejection of claim 10 be reversed for this additional reason.

Claim 21

Claim 21 recites *a method of calibrating a device that includes a controllable oscillator and a resonating device that supplies a fixed frequency used by the controllable oscillator to synthesize an output clock.* The Office action relies on column 3, lines 60-63, of Walker to teach a resonating device. Walker teaches at col. 3, lines 60-67 that a transmitted reference signal such as a horizontal sync or color burst pulse inherent in a broadcast television signal can be used for controlling the master clock to operate with an improved range of accuracy. Walker fails to teach a resonating device as claimed. Accordingly, Applicants respectfully request that the rejection of claim 21 be reversed for this additional reason.

Claim 42

Claim 42 recites a *resonating device supplying a reference signal having a fixed frequency* coupled to the controllable oscillator. The Office action states that Walker teaches in

column 3, lines 60-63, a fixed frequency reference source to synthesize the output clock. Walker teaches at col. 3, lines 60-67 that a transmitted reference signal such as a horizontal sync or color burst pulse inherent in a broadcast television signal can be used for controlling the master clock to operate with an improved range of accuracy. Walker does not teach a resonating device having a fixed frequency. There is no resonating device shown in Walker supplying a fixed frequency to the controllable oscillator. A transmitted reference signal such as a horizontal sync or color burst pulse inherent in a broadcast television signal of Wilson does not teach a resonating device having a fixed frequency. Accordingly, Applicants respectfully request that the rejection of claim 42 be reversed for this additional reason.

Ground II: The rejection of claims Claims 3-5, 20, and 44-47 under 35 U.S.C. § 103(a) as being unpatentable over Walker et al. in view of Sutardja (U.S. Pub. 2004/0071029).

Claim 3-5,44-47

Claims 3-5, 20, and 44-47 are rejected under 35 U.S.C. § 103(a) as being obvious over Walker et al. in view of Sutardja.

In general, obviousness is a legal determination based on underlying factual inquiries. See Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc., 976 F.2d 1559, 1572-73, 24 USPQ2d 1321, 1332-33 (Fed. Cir. 1992). Graham v. John Deere Co., 383 U.S. 1, 17 (1966) defines the factual inquiries utilized to evaluate the prior art. Specifically, the prior art is evaluated in terms of: (1) its scope and content; (2) the differences between the prior art and the claimed invention; (3) the level of ordinary skill in the art at the time the application was filed; and (4) objective, or secondary, evidence of nonobviousness such as commercial success, failure of others, long-felt need and unexpected results, which must be considered in reaching a conclusion of obviousness. See Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 460 (1966); Panduit Corp. v. Dennison Mfg. Co., 810 F.2d 1561, 1566-67, 1 USPQ2d 1593, 1595-96 (Fed. Cir. 1987); Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc., 976 F.2d 1559, 1573, 24 USPQ2d 1321, 1333 (Fed. Cir. 1992).

In the present appeal the issue for claims 3-5, and 47 relates to whether the combination of Sutardja and Walker is proper.

> Most inventions arise from a combination of old elements and each element may often be found in the prior art. [In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457 (Fed. Cir. 1998)] However, mere identification in the prior art of each element is insufficient to defeat the patentability of the combined subject matter as a whole. *Id.* at 1355, 1357. Rather, to establish a *prima facie* case of obviousness based on a combination of elements disclosed in the prior art, the Board must articulate the basis on which it concludes that it would have obvious to make the claimed invention. *Id.* In practice, this requires that the Board "explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious."
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> In re Kahn, 441 F.3d 977, 986, 78 USPQ2d 1329, 1335 (Fed. Cir. 2006).

Claim 3 recites *generating at least a second control value using the phase-locked loop to lock the clock generated by the controllable oscillator to a multiple of the calibration clock and wherein the at least one control value and the second control value are generated at first and second temperatures*. Claim 47 recites *generating a second control value using the control loop to lock the clock generated by the controllable oscillator to a multiple of the calibration clock, wherein the control value and the second control value are generated at first and second temperatures; and storing a second value associated with the second control value in the nonvolatile memory.*

The final Office action relies on the combination of Walker and Sutardja to teach claims 3-5 and 44-47. The final Office action states it would have been obvious to combine Sutardja with Walker because "it would have been obvious to one of ordinary skill in the art at the time of the invention to utilize such temperature value storing in a NVM because such a modification would have provided the benefit of temperature compensation for more stable clock frequency." Applicants respectfully disagree that it would be obvious to combine the teachings of Sutardja with Walker because the temperature compensation in Sutardja is not needed or useful in Walker. In Sutardja, temperature compensation is necessary for a precision frequency reference circuit formed by a semiconductor oscillator (instead of, e.g., a crystal). Semiconductor oscillators can have excessive variation in the oscillating frequency, especially with temperature changes, and thus need temperature compensation to be effective. See Sutardja, paragraph 0004.

However, Walker does not teach a precision frequency reference source. Instead, Walker teaches a circuit that is intended to recover timing in received signals. Walker, col. 3, lines 45-67. The master clock output rate control in Walker is transferred to the timing component embedded in the received signals after an initial calibration that is used to get the master clock close to the timing component. Walker, col. 4, lines 34-38. There is no reason to compensate for temperature during calibration because the initial calibration is intended only to get the master clock close to the timing embedded in the received data. Additionally, there is no reason to compensate for temperature after calibration since the circuit of Walker is intended to track the timing of the received signal on 10 and the temperature is irrelevant.

The Examiner, while stating it would provide "a more stable clock frequency," has not explained how Walker could exploit temperature compensation. Walker initially adjusts the master clock 20 to be close to the timing of the received data 10 and then acquires the timing embedded in the received data. Applicants respectfully submit that it would be illogical for Walker to adjust the master clock 20 at two different temperatures and then acquire the timing embedded in the received data. The point of Walker is to reduce the acquisition time of a desired information signal. Col. 6, lines 26-28. Adjusting the master clock at two different temperatures and storing the control values would increase the acquisition time. Such temperature compensation simply makes little sense in Walker. Accordingly, Applicants submit that there is no motivation at all to modify Walker to store *the at least one control value and the second control value generated at first and second temperatures.* Accordingly, absent motivation to modify Walker with the temperature compensation of Sutardja, claims 3-5 and 44-47 distinguish over the references of record. Therefore, the Board is requested to reverse the rejection of claims 3-5, and 44-47.

Claim 20

With respect to claim 20, the Office action states that "disabling a temperature compensation mode of operation prior to providing the calibration clock would have been obvious based on the consideration of controlling variations." The Applicants respectfully submit, given the discussion of claim 3 above, that there is no proper combination teaching modifying Walker to have temperature compensation. Accordingly, it cannot be obvious to

disable a mode that is not in Walker. Therefore, the Board is requested to reverse the rejection of claim 20.

Ground III: The rejection of claims 11-15, 18, 20, 23-25, 29-41, 43 and 48 under 35 U.S.C. § 103(a) as being unpatentable over Walker et al. in view of Torode (U.S. Patent No. 5,451,912).

Claims 11-15, 18, 20, 23-25, 29-41, 43 and 48 are patentable for the reasons that they directly or indirectly depend on independent claims that are patentable over Walker. Accordingly, Applicants submit that a prima facie case of obviousness has not been made for any of these dependent claims. Additional reasons for patentability for certain of the claims rejected under Ground III are argued below.

Claims 13-15, 24-25, 29

Claims 13-15, 24-25, and 29 recite limitations that are not taught in the prior art, alone or in combination. All claim limitations must be considered in the obviousness analysis. Indeed, it is clear error to ignore limitations clearly set forth in the claims. See Panduit Corp., 810 F.2d at 157, 61 USPQ2d at 1603 – 04. None of the references, standing alone or in combination, teach all of the recited limitations in this group of claims.

Claim 13 recites *receiving at least one command sequence over the terminal prior to receiving a calibration clock.* The terminal is the terminal over which the calibration clock is received in claim 1. That capability is illustrated, e.g., with respect to Fig. 3 of the instant application, where the command(s) to set up the calibration and the calibration clock are received over node 27. There is no such teaching in Walker or Torode. Nor has the Examiner pointed to such a teaching. In Torode, there is no calibration clock supplied. Instead, a test vector is supplied, and it is determined if the test vector generates a desired output frequency. See Torode, col. 7, lines 45-57. In Walker no commands are used. There is simply no teaching of the claimed limitation in Walker or Torode, alone or in combination. With respect to claims 13-15, Applicants respectfully submit that the Examiner has not established a prima facie case of obviousness since the references fail to teach all the claim limitations. Accordingly, Applicants respectfully request that the rejection of claims 13-15, 24-25, and 29 be reversed.

Similarly, with regards to claims 24-25, Applicants submit that there is no teaching in the Walker or Torode, alone or in combination regarding receiving at least one command sequence over the input/output terminal prior to receiving the calibration clock over the input/output terminal. Accordingly, Applicants respectfully request that the rejection of claims 24 and 25 be reversed.

Similarly, with respect to claim 29, there is no teaching that the apparatus is coupled to respond to input signals on the terminal (on which it receives a calibration clock signal) as serial commands. Accordingly, Applicants respectfully request that the rejection of claim 29 be reversed.

Claims 15, 32, 41

The issue for claims 15, 32 and 41 relates to specific differences between the prior art and appealed claims. None of the references, standing alone or in combination, teach all of the recited limitations.

With respect to claims 15, 32, and 41, the Applicants respectfully submit that the Examiner is mistaken as to the teachings of Walker. Claim 15 recites that *the terminal* (over which the calibration clock is received) *is bidirectional and a serial command received over the terminal is a read command causing data to be provided on the terminal.* The Office action argues that Fig. 1 of Walker shows terminal 50 being bi-directional. That is incorrect. Fig. 1 shows terminal 50 is coupled to a switch and based on the switch setting can be coupled to a transmitted reference 34 or to the symbol timing loop 40 that also supplies the symbol timing to packet ID detector 12. The teaching of Walker is in fact that terminal 50 is uni-directional. The signals on terminal 50 go in only one direction (into the calibration loop). While there is a switch allowing a source to vary, it is still uni-directional. In contrast bi-directional terminals allow information to be written and read from the integrated circuit being calibrated. No such bi-directional capability is shown in Walker. Accordingly, Applicants respectfully request that the rejection of claims 15, 32, and 41 be reversed.

Claim 18

Claim 18 recites setting a voltage control input to midrange prior to providing the calibration clock. With reference to Fig. 4, the voltage control in put on node 43 would affect the DCO output and thus calibration if not set to midrange. The Office Action states simply that it would have been obvious "based on the optimization range." Applicants do not understand to what optimization range in Torode or Walker the Examiner is referring. There is no such voltage control input in Walker or Torode. Since the references fail to teach the element, a prima facie case of obviousness has not been established. Accordingly, Applicants respectfully request that the rejection of claim 18 be reversed.

Claim 20

Claim 20 recites *disabling a temperature compensation mode of operation prior to providing the calibration clock.* With respect to claim 20, the Office action states that "disabling a temperature compensation mode of operation prior to providing the calibration clock would have been obvious based on the consideration of controlling variations." The Applicants respectfully submit, given the discussion of claim 3 above, that there is no proper combination that teaches modifying Walker to have temperature compensation. Accordingly, it cannot be obvious to disable a mode that is not in Walker. Accordingly, Applicants respectfully request that the rejection of claim 20 be reversed.

CONCLUSION

For the foregoing reasons, Appellants' respectfully submit that claims 1-7 and 10-48 distinguish over Walker, Sutardja, and Torode, alone or in combination. Accordingly, the Board is respectfully requested to reverse the rejections of claims 1-7 and 10-48 and to direct the claims of the present application to be issued.

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Respectfully submitted,

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CLAIMS APPENDIX

1. (Previously presented) A method comprising:
receiving a calibration clock over a terminal;
generating at least one control value in a control loop to lock a clock generated by a controllable oscillator to a multiple of the calibration clock; and
storing a value corresponding to the at least one control value in a non volatile memory.

2. (Original) The method as recited in claim 1 wherein the control loop is a phase-locked loop.

3. (Previously presented) The method as recited in claim 2 further comprising generating at least a second control value using the phase-locked loop to lock the clock generated by the controllable oscillator to a multiple of the calibration clock and wherein the at least one control value and the second control value are generated at first and second temperatures.

4. (Original) The method as recited in claim 3 further comprising storing the first and second temperatures in the non-volatile memory.

5. (Previously presented) The method as recited in claim 3 further comprising storing a difference between the at least one control value at the first temperature and the second control value at the second temperature.

6. (Previously presented) The method as recited in claim 2 further comprising determining if the phase-locked loop is locked to the calibration clock during receipt of the calibration clock.

7. (Original) The method as recited in claim 1 wherein the multiple is one of an integer multiple and fractional multiple of the calibration clock.

8. (Canceled)

9. (Canceled)

10. (Previously presented) The method as recited in claim 1 further comprising supplying a fixed frequency reference from a fixed frequency reference source to synthesize the clock.

11. (Original) The method as recited in claim 10 wherein the fixed frequency reference source is one of a crystal and a surface acoustic wave (SAW) device.

12. (Original) The method as recited in claim 10 further comprising receiving the calibration clock while the nonvolatile memory, fixed frequency reference source and the phase-locked loop are in a sealed package.

13. (Original) The method as recited in claim 1 further comprising receiving at least one command sequence over the terminal prior to receiving the calibration clock.

14. (Original) The method as recited in claim 13 wherein the at least one command sequence programs a storage location and determines a divider value utilized by a divider circuit in the phase-locked loop according to a value in the storage location.

15. (Original) The method as recited in claim 13 wherein the terminal is bidirectional and a serial command received over the terminal is a read command causing data to be provided on the terminal.

16. (Original) The method as recited in claim 2 further comprising selectively coupling the controllable oscillator to a feedback path to form the phase-locked loop.

17. (Original) The method as recited in claim 1 wherein the controllable oscillator is supplied a digital control value.

18. (Original) The method as recited in claim 1 further comprising setting a voltage control input to midrange prior to providing the calibration clock.

19. (Original) The method as recited in claim 1 further comprising disabling a voltage controlled crystal oscillator (VCXO) mode of operation prior to providing the calibration clock.

20. (Original) The method as recited in claim 1 further comprising disabling a temperature compensation mode of operation prior to providing the calibration clock.

21. (Previously presented) A method of calibrating a device that includes a controllable oscillator and a resonating device that supplies a fixed reference frequency used by the controllable oscillator to synthesize an output clock, the controllable oscillator and the resonating device being mounted in a package, the method comprising:

supplying a calibration clock to an input/output terminal of the device;

generating a control value in a control loop of the device to cause the controllable oscillator to lock to a multiple of the calibration clock; and

storing a value determined according to the control value in a non-volatile memory in the device.

22. (Previously presented) The method as recited in claim 21 wherein a phase-locked loop is selectively implemented as the control loop and includes the controllable oscillator and generates the control value during calibration.

23. (Original) The method as recited in claim 21 wherein the resonating device is one of a crystal and a surface acoustic wave (SAW) device.

24. (Original) The method as recited in claim 21 further comprising receiving at least one command sequence over the input/output terminal prior to receiving the calibration clock.

25. (Original) The method as recited in claim 24 wherein the at least one command sequence determines a divider value utilized by a divider circuit in a phase-locked loop generating the control value during calibration, the divider value being determined according to a value in the storage location.

26. (Previously presented) An apparatus comprising:

a controllable oscillator coupled to receive a reference frequency and a control value and to output a clock signal;

a terminal for receiving a calibration clock signal;

a phase-locked loop circuit including the controllable oscillator is coupled to receive the calibration clock signal and generate a correction factor to cause the controllable oscillator to lock to a multiple of the calibration clock signal ; and

a non-volatile memory storing a value corresponding to the correction factor.

27. (Original) The apparatus as recited in claim 26 wherein the controllable oscillator is selectively coupled as part of the phase-locked loop.

28. (Previously presented) The apparatus as recited in claim 26 further comprising memory locations storing a history of correction factors determined during calibration of the apparatus.

29. (Original) The apparatus as recited in claim 26, wherein the apparatus is further coupled to respond to input signals on the terminal as serial commands.

30. (Original) The apparatus as recited in claim 26 wherein the apparatus is an integrated circuit.

31. (Original) The apparatus as recited in claim 26 wherein the terminal is a pin on a package holding a semiconductor device.

32. (Original) The apparatus as recited in claim 26 wherein the terminal is bi-directional.

33. (Original) The apparatus as recited in claim 26, further comprising an integrated circuit including a control circuit coupled to determine when the terminal has had a particular value for longer than a predetermined time period, and to supply an internal output enable signal

having the particular value to selectively enable the one or more clock signals according to the particular value.

34. (Original) The apparatus as recited in claim 33 wherein transitions on the terminal that occur in less than the predetermined time period are determined to be serial data communication signals.

35. (Original) The apparatus as recited in claim 26, further comprising an integrated circuit including the controllable oscillator and the phase-locked loop.

36. (Original) The apparatus as recited in claim 35 wherein the apparatus includes a resonating device supplying the reference frequency and a package holding the resonating device and the integrated circuit.

37. (Original) The apparatus as recited in claim 36 wherein the resonating device is one of a crystal and a surface acoustic wave (SAW) device.

38. (Original) The apparatus as recited in claim 26 wherein a serial command sent to the input terminal is utilized to communicate to the apparatus that the calibration clock is going to be supplied.

39. (Original) The apparatus as recited in claim 36 wherein the package is a ceramic package.

40. (Original) The apparatus as recited in claim 33 wherein when the terminal is used as a serial data port, data transitions on the terminal occur at less than the predetermined interval and the data transitions do not change a current value of the internal output enable signal.

41. (Original) The apparatus as recited in claim 40 wherein the serial data port is bi-directional.

42. (Previously presented) An apparatus comprising:

a terminal for receiving a signal;

a resonating device supplying a reference signal having a fixed frequency;

a controllable oscillator coupled to receive the reference signal and generate a clock signal;

means for calibrating the apparatus utilizing a calibration clock supplied on the terminal by internally generating, in a phase-locked loop, one or more control values for the controllable oscillator to cause the oscillator to output a signal corresponding to the calibration clock; and

a non-volatile storage storing one or more values corresponding to the one or more control values.

43. (Original) The apparatus as recited in claim 42 wherein the apparatus comprises an integrated circuit and a resonating device in a sealed package.

44. (Previously presented) The apparatus as recited in claim 42 wherein the means for calibrating further generates at least a second control value using the phase-locked loop to lock the clock generated by the controllable oscillator to a multiple of the calibration clock and wherein the one control value and the second control value are generated at first and second temperatures.

45. (Previously presented) The apparatus as recited in claim 44 wherein the first and second temperatures are stored in the non-volatile storage.

46. (Previously presented) The apparatus as recited in claim 44 wherein a difference between the at least one control value at the first temperature and the second control value at the second temperature is stored in the non-volatile storage.

47. (Previously presented) The method as recited in claim 21 further comprising:

generating a second control value using the control loop to lock the clock generated by the controllable oscillator to a multiple of the calibration clock, wherein the

control value and the second control value are generated at first and second temperatures; and

storing a second value associated with the second control value in the nonvolatile memory.

48. (Previously presented) A device including an integrated circuit calibrated according to the method of claim 47.

EVIDENCE APPENDIX

There is no evidence submitted pursuant to 37 C.F.R. § 1.130, 1.131, or 1.132 or any other evidence entered by the examiner and relied upon by appellant in the appeal.

RELATED APPEALS APPENDIX

There are no decisions rendered by a court or the Board in any proceeding identified above in the Related Appeals and Interferences section.